AMENDMENTS TO THE DRAWINGS:

Attached to this Amendment is a replacement Figure 2 in order to delete reference number 0.

REMARKS

This Amendment responds to the Office Action dated March 2, 2005 in which the Examiner objected to the drawings and rejected claims 1-4 and 10-11 under 35 U.S.C. §103.

Attached to this Amendment is a replacement sheet in which reference numeral 0 is deleted from Figure 2. Applicants respectfully request the Examiner approves the correction.

Claim 1 claims a semiconductor light emitting device comprising a mesa section and an inorganic insulating film. The mesa section has at least a sandwich structure of an n-type clad layer, an active layer and a p-type clad layer which are constituted by compound semiconductor layers formed on a substrate. The inorganic insulating film is formed to cover the mesa section excluding a contact region. The inorganic insulating film is constituted by an inorganic insulating film having a vacancy rate of 50% or more.

Through the structure of the claimed invention having an inorganic insulating film having a vacancy rate of 50% or more, as claimed in claim 1, the claimed invention provides a semiconductor light emitting device having a reduced pad capacity and increased modulating speed. The prior art does not show, teach or suggest the invention as claimed in claim 1.

Claims 1-4 and 10-11 were rejected under 35 U.S.C §103 as being unpatentable over *Iwano et al.* (U.S. Patent No. 5,621,750) in view of *Mandal* (U.S. Patent No. 6,559,070).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for

reasons which will be set forth below, Applicants respectfully request the Examiner withdraws the rejection to claims and allows the claims to issue.

Iwano et al. appears to discloses a surface emission type semiconductor laser for emitting light in a direction perpendicular to the plane of a substrate. (Col. 1, lines 8-10) As shown in FIG. 1, the semiconductor laser 100 comprises a substrate 102 of n-type GaAs, a distributed-Brag reflection type multilayer film mirror (hereinafter called "DBR mirror") 103 including 40 pairs of an n-type $Al_{0.8}$ $Ga_{0.2}$ As layer and an n-type $Al_{0.15}$ $Ga_{0.85}$ As layer alternately deposited one above another, and having a reflectivity of 99.5% or more relative to light having a wavelength equal to about 800 nm, a first clad layer 104 of n-type $Al_{0.7}$ $Ga_{0.3}$ As, a quantum well active layer 105 (which is of multiple quantum well (MQW) structure in this embodiment) including twenty-one pairs of an n^--type GaAs well layer and an n^--type $Al_{0.3}$ $Ga_{0.7}$ As barrier layer, a second clad layer 106 of p-type $Al_{0.7}$ $Ga_{0.3}$ As and a contact layer 109 of p^+-type $Al_{0.15}$ $Ga_{0.85}$ As, these layers being sequentially deposited on the substrate 102 in such an order as described. The contact layer 109 and the upper portion of the second clad layer 106 are etched into a cylindrical column-like portion 114 (hereinafter called "resonator portion", the resonator portion need not necessarily be cylindrical as will be explained later in this text). The resonator portion 114 is buried with a first insulation layer 107 of silicon oxide film (SiO_x film) such as SiO_2 or the like and a second insulation layer 108 of heat-resistant resin such as polyimide or the like. (Col. 14, lines 44-67) The first insulation layer 107 formed of silicon oxide film (SiO_x film) shown in FIG. 1 has a film thickness of 500 to 2000 Angstroms. The second insulation layer 108 of heat-resistant resin or the like is required to flatten the surface of the element. However, for example, when heat-resistant resins is used

heat-resistant resins tend to include residual moisture in the film, and when an element is operated for a long time while such a heat-resistant resin is in direct contact with the semiconductor layer, voids will be produced at the interface between the heat-resistant resin and the semiconductor layer to degrade the characteristics of the element. When a thin film such as the first insulation layer 107 is inserted into the interface between the heat-resistant resin and the semiconductor layer according to one embodiment, the first insulation layer 107, in addition to other advantages, serves as a protective film to prevent such a degradation. (Col. 15, line 55 through Col. 16, line 3)

Thus, *Iwano et al.* merely discloses a heat-resistant resin which when heated and in direct contact with a semiconductor layer will produce voids at the interface between the heat-resistant resin and the semiconductor layer (col. 15, lines 60-65). Nothing in *Iwano et al.* shows, teaches or suggests an inorganic insulating film having a vacancy rate of 50% or more as claimed in claim 1. Rather, *Iwano et al.* teaches away from the claimed invention since voids are formed at the interface between the resin and semiconductor layer.

Additionally, *Iwano et al.* merely discloses inserting an insulation layer 107 between the heat resistive resin and the semiconductor layer to prevent degradation caused by the voids. (Col. 15, line 66 through col. 16, line 3). Thus nothing in *Iwano et al.* shows, teaches or suggests an inorganic insulating film having a vacancy rate of 50% or more as claimed in claim 1. In fact, *Iwano et al.* teaches away from having a vacancy rate since the insulating layer 107 is inserted in order to prevent degradation caused by voids between a heat-resistant resin and a semiconductor layer and thus would be free of voids.

Mandal appears to disclose a process for depositing dielectric layers on a substrate. (Col. 1, lines 8-9) In order to further reduce the size of devices on integrated circuits, it has become necessary to use conductive materials having low resistivity and insulators having low dielectric constants (k, wherein k<4.0) to reduce the capacitive coupling between adjacent metal lines. (Col. 1, lines 20-24) There remains a need for a process to deposit ion diffusion resistant low k dielectric materials with high substrate throughput. (Col. 3, lines 13-15) A method and apparatus are provided for depositing a mesoporous silicon oxide layer having a low dielectric constant. In accordance with one aspect a process is provided for depositing a mesoporous oxide layer having a low dielectric constant and a high phosphorus content. (Col. 5, lines 26-31) The mesoporous oxide film will have a porosity of al least 50% and a dielectric constant between about 1.6 and about 2.2. The mesoporous film may also be used as a inter-metal dielectric layer. It is believed that the phosphorus doping advantageously provides the combined benefits of ion mobilization, acceleration of deposited hydrolysis completion and condensation, and improved film strength. (Col. 5, lines 45-52)

Thus, *Mandal* merely discloses a mesoporous film having a porosity of at least 50%. Applicants respectfully submit that *Mandal* cannot be combined with *Iwano et al.* since *Iwano et al.* clearly teaches using an insulating film 107 in order to prevent degradation caused by voids whereas *Mandal* teaches a film having voids. Furthermore, the references cannot be combined, since Applicants respectfully submit that a person of skill in the art would not look to *Mandel* which discloses a porous material in order to stop the degradation in *Iwano et al.*, which discloses having voids at the interface between a resin and semiconductor layer. Therefore,

Applicants respectfully submit that the combination of *Iwano et al.* and *Mandal* is not possible. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claim 1 under 35 U.S.C. §103.

Claims 2-4 and 10-11 depend from claim 1 and recite additional features. Applicants respectfully submit that claims 2-4 and 10-11 would not have been obvious within the meaning of 35 U.S.C. §103 over *Iwano et al.* and *Mandal* at least for the reasons as set forth above. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 2-4 and 10-11 under 35 U.S.C. §103.

The prior art of record, which is not relied upon, is acknowledged. The references taken singularly or in combination do not anticipate or make obvious the claimed invention.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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